

*We claim:*

1. A process for fabricating a leadless plastic chip carrier, comprising the steps  
5 of:

depositing a mask on a first surface of a leadframe strip to define at least one row of contact pads and a power/ground ring adjacent a die attach pad of said leadless plastic chip carrier;

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depositing a plurality of layers on portions of said surface exposed by said mask for creating said at least one row of contact pads, said power/ground ring and said die attach pad;

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dissolving away said mask;

mounting a semiconductor die to said die attach pad on said top surface and wire bonding said semiconductor die to said contact pads;

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encapsulating said top surface of said leadframe strip in a molding material;

etching back a bottom surface of said leadframe strip for exposing said contact pads and said die attach pad; and

singulating said leadless plastic chip carrier from said leadframe strip.

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2. The process of claim 1, wherein said step of depositing said plurality of layers includes an initial deposition of flash Cu which is etched away during step of etching back said bottom surface to create a cavity, and further including a step of attaching

solder balls to said contact pads exposed as a result of said step of etching back said bottom surface of said leadframe strip.

3. The process of claim 2, wherein said initial deposition of flash Cu is followed  
5 by depositing layers of Au, Ni, Cu, Ni and Au.

4. The process of claim 2, wherein said initial deposition of flash Cu is followed  
by depositing layers of Au, Ni, Cu and Ag.

10 5. The process of claim 1, wherein said step of depositing said plurality of layers  
includes depositing successive layers of Au, Ni, Cu, Ni and Au.

6. The process of claim 1, wherein said step of depositing said plurality of layers  
includes depositing successive layers of Au, Ni, Cu, and Ag.

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7. The process of claim 1, wherein said step of depositing said plurality of layers  
includes depositing successive layers of Tin, Cu, Ni and Au.

8. The process of claim 1, wherein said step of depositing said plurality of layers  
20 includes depositing successive layers of Tin, Cu, and Ag.

9. A leadless plastic chip carrier, comprising:

a semiconductor die mounted to a ground plane;

at least one row of contact pads circumscribing said ground plane;

a power/ground ring intermediate said at least one row of contact pads and said ground plane;

a plurality of wire bonds connecting various ones of said semiconductor die,  
5 said power/ground ring and said row of contact pads; and

an overmold covering said semiconductor die and all expect one exposed surface of said row of contact pads and said ground plane.

10. The leadless plastic chip carrier of claim 9, wherein said at least one row of  
10 contact pads comprises a plurality of metal layers deposited to form a rivet shape in profile.

11. The leadless plastic chip carrier of claim 9, wherein said at least one row of  
contact pads is round.

12. The leadless plastic chip carrier of claim 9, wherein said at least one row of  
15 contact pads is rectangular.

13. The leadless plastic chip carrier of claim 9, wherein said at least one row of  
20 contact pads is recessed into said overmold to form a plurality of etch down cavities.

14. The leadless plastic chip carrier of claim 13, further including a plurality of solder balls within said etch down cavities and connected to said at least one row of contact pads.

15. The leadless plastic chip carrier of claim 1, wherein an outer edge of said ground plane conforms to an interlock pattern.

16. The leadless plastic chip carrier of claim 10, wherein said plurality of metal  
5 layers comprises successive layers of Au, Ni, Cu, Ni and Au.

17. The leadless plastic chip carrier of claim 10, wherein said plurality of metal layers comprises successive layers of Au, Ni, Cu, and Ag.

10 18. The leadless plastic chip carrier of claim 10, wherein said plurality of metal layers comprises successive layers of Tin, Cu, Ni and Au.

19. The leadless plastic chip carrier of claim 10, wherein said plurality of metal layers comprises successive layers of Tin, Cu, and Ag.

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20. The leadless plastic chip carrier on claim 10 wherein the etched strip is passed through a hot air level soldering step to coat the external metal surfaces with a thin uniform layer of solder.